Demonstration of reliable memory operation in the world's smallest 1 Selector-1 MTJ cell

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We demonstrate 1 Selector-1 MTJ (1S1M) cell operation in the world's highest-density 64 Gb cross-point STT-MRAM chips. We have achieved Half Pitch (HP) of 20.5 nm and MTJ Critical Dimension (CD) of 20 nm using As doped SiO2 selector and perpendicularly magnetized MTJ (p-MTJ). A novel read scheme utilizing transient behavior of selector along with the low capacitance circuitry enables us to overcome MTJ read disturbance which typically occurs when the selector turns on in scaled 1S1M cells.

***Index Terms*—MRAM, Selector, Crosspoint architecture, Read disturbance**

I. Introduction

NOVEL applications such as AI and big data processing are driving the growth of an enormous market. To further accelerate this growth, the long-awaited arrival of storage-class memory (SCM) with high performance and high bit density is essential. STT-MRAM (Spin Transfer Torque Magnetic Random Access Memory) is a promising candidate for next-generation non-volatile memory. We previously presented 4 Gb STT-MRAM with $9F^2$ 1 transistor-1 MTJ cells in 2016 [1]. However, transistors as three-terminal select devices pose challenges for increasing bit density due to their poor drivability for write operation and the complexity of contact plug layout. Recently, 1 selector-1 MTJ (1S1M) cell, comprising two-terminal select device and MTJ has been proposed to shrink cell size toward $4F^2$ [2-4]. Although low read disturbance was demonstrated in relatively large MTJ CD of 60 nm for high-density embedded memory [4], shrinking MTJ with maintaining low disturbance remains to be done.

In this work, we demonstrate 1S1M cell operation in the world's highest-density 64 Gb cross-point STT-MRAM chips [5]. We have achieved HP of 20.5 nm and MTJ CD of 20 nm using As doped SiO2 selector and perpendicularly magnetized MTJ (p-MTJ). A novel read scheme utilizing transient behavior of selector along with the low capacitance circuitry enables us to overcome MTJ read disturbance which typically occurs when the selector turns on in scaled 1S1M cells.

II. Structure of 1S1M Cells

Figure 1 shows the cross-sectional TEM images of 64 Gb cross-point MRAM test chip. To minimize the chip size, CMOS circuitry is integrated underneath 1S1M cell array. The CMOS circuitry contains row and column select switches (SW), a write driver (W/D) and a sense amplifier (S/A).

The cell array consists of word-line (WL), bit-line (BL) and 1S1M cells with HP of 20.5 nm. The 1S1M cells have As-doped SiO2 selector and p-MTJ. 4K (2K) cells are connected to BL (WL). At every cross point, 1S1M cell is sandwiched between BL and WL to make up an 8 Mb MAT. Finally, the world's smallest cell, measuring 0.001681 um^2, has been achieved with $4F^2$ design. The key features of the test chip are summarized in Table 1.

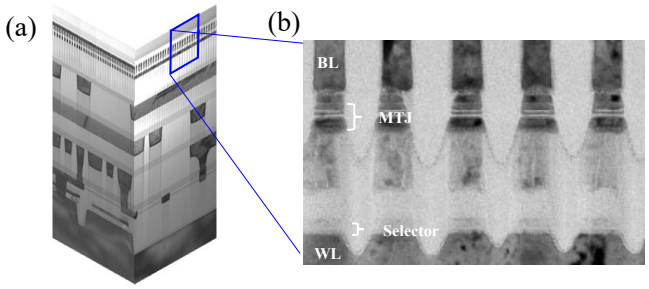

Fig. 1. 64 Gb cross-pint MRAM architecture. (a) Cross sectional TEM image. (b) 1S1M array [5].

TABLE I
Key Features of the Test Chip [5]

Item	Specification
Tech node	20.5 nm
Density	64 Gb
MAT size	4096-Rows and 2048-Columns
Read speed	6~10 nsec
Write speed	15~30 nsec

III. MTJ Characteristics

The resistance-field (R-H) curve and write error rate (WER) of typical 20 nm MTJ with HP 20.5 nm are shown in Figure 2(a) and (b), respectively. For comparison, the data of previous HP 22.5 nm MTJ [2] are also included. From self-fluctuation of magnetic coercivity (H_c), thermal stability factor (Δ) is estimated to be greater than 60 at 90℃. Despite extensive modifications to the MTJ and its fabrication process, MTJ data retention and WER have been maintained while reducing HP from 22.5 nm to 20.5 nm.

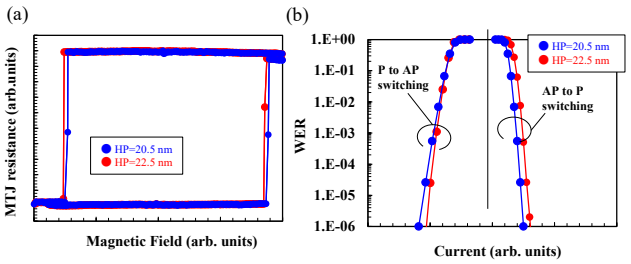

Fig. 2. Typical MTJ properties of HP 20.5 nm (blue dot) and 22.5nm (red dot). (a) R-H curve of a single MTJ device. (b) Write Error Rate (WER) at write pulse duration of 15 nsec [5].

IV. 1S1M Cell Operation

Reducing read disturbance is one of the most critical challenges in high-density 1S1M architecture. As MTJ CD shrinks, read current must be reduced to suppress unintentional writing, known as read disturbance. However, the selector holding current, which is necessary to prevent selector on/off oscillation, is typically much higher than the required read current, especially in scaled 1S1M cells. Additionally, the large spike current generated during selector turn-on operation further excerbates read disturbance. To address this issue, a novel read scheme utilizing transient behavior of selectors along with the low capacitance circuitry has been implemented in our test chip. The circuitry is pre-charged before selector turn-on, and the release of a spike current in a short duration right after the turn-on is utilized for read operation.

Figure 3 shows the simulated time evolution of the cell current from selector turn-on to turn-off. In high-cap mode, where the circuitry has a large capacitance component, a large amount of charge flows, leading to severe read disturbance. Conversely, in low-cap mode, the capacitance component is minimized, making the cell current decay faster to effectively suppress read disturbance. Figure 4(a) shows the external field response of readout signal for a typical 1S1M cell. In high-cap mode, only AP state can be maintained at zero magnetic field due to large cell current at reading operation, whereas bi-stable state of AP and P can be read in low-cap mode. Figure 4(b) shows the read disturbance test by monitoring 1S1M readout signal under cyclic read stress. No read disturbance was observed at least up to 1E6 read cycle in low-cap mode.

Finally, cyclic read/write operation was tested for a typical 1S1M cell as shown in Figure 5. The extrapolated read/write error rate reaches approximately -5σ (<1E-6), demonstrating the effectiveness of the novel read scheme with low-cap mode in suppressing read disturbance.

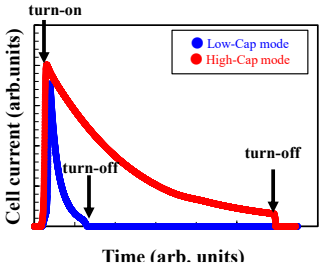

Fig. 3. Simulation results of cell current evolution from selector turn-on to turn-off, on low capacitance circuitry (blue line) and high capacitance circuitry (red line) [5].

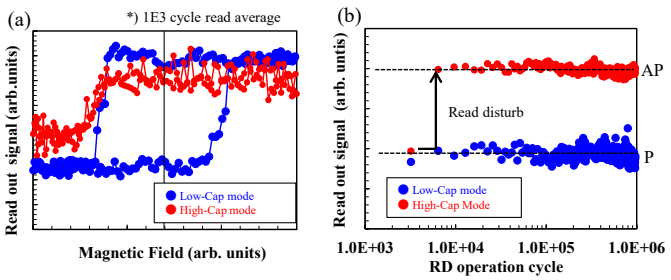

Fig. 4. (a) External magnetic field response of 1S1M cell, on low capacitance circuitry (blue dots) and high capacitance circuitry (red dots). (b) The result of read disturbance test by applying cycling read-only stress [5].

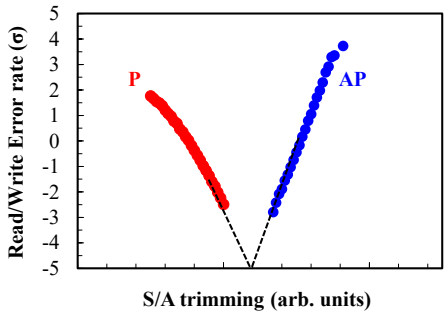

Fig. 5. Cyclic read/write operation test result for a typical 1S1M cell. Test sequence is up to 1E3 cycle consecutive "Reset (0/1) > Read > Write (1/0) > Read" operation at each S/A trimming condition. The extrapolated read/write error rate reaches around -5σ (<1E-6) [5].

V. Conclusion

We have successfully achieved the world's smallest 1S1M cell, measuring 0.001681 um^2, by incorporating optimized material design and fabrication process technologies. Furthermore, reliable 1S1M read/write operation with error rate of <1E-6 has been demonstrated. To achieve this low error rate, the novel read scheme utilizing transient behavior of selector along with the low capacitance circuitry plays a critical role in reducing read disturbance, which remains one of the most essential technical challenges for cross-point 1S1M architecture. We believe our work represents a significant leap toward high-density, high-performance, and highly reliable cross-point MRAM for SCM applications.

References

[1] S.-W. Chung et al., "4Gbit density STT-MRAM using perpendicular MTJ realized with compact cell structure" *IEDM Tech. Digest,* pp.659-662, 2016.

[2] S.M. Seo et al., "First demonstration of full integration and characterization of 4F2 1S1M cells with 45 nm of pitch and 20 nm of MTJ size", *IEDM Tech. Digest*, pp.218-221, 2022.

[3] H. Yang et al., "Threshold Switching Selector and 1S1R Integration Development for 3D Cross-point STT-MRAM", *IEDM Tech. Digest*, pp.836-839, 2017.

[4] E. Ambrosi et al., "Low voltage (<1.8 V) and high endurance (>1M) 1-Selector/1-STT-MRAM with ultra-low (1 ppb) read disturb for high density embedded memory arrays", *IEDM Tech. Digest*, 21-5, 2023.

[5] H. Aikawa et al., "Reliable memory operation with low read disturb rate in the world smallest 1Selector-1MTJ Cell for 64 Gb cross-point MRAM," *IEDM Tech. Digest*, 20-1, 2024.