Magnetic Ordered Alloy based Free Layer materials for high-speed writing of MRAM devices with high retention

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In this study we are discussing new materials options for STT-MRAM free layer materials beyond CoFeB films with perpendicular interface anisotropy. We demonstrate the growth and integration of low moment and high bulk perpendicular magnetic anisotropy ordered alloy films on CMOS wafers. Novel device properties such as high retention ($E_b > 80k_BT$), high device coercivity ($H_c > 8kOe$) and reliable switching down to 2ns write times are obtained simultaneously.

Index Terms- High retention MRAM, High perpendicular magnetic anisotropy, Ordered magnetic alloy, STT-MRAM

I. INTRODUCTION

Perpendicular anisotropy for STT-MRAM free layer materials has typically been relying on the CoFeB|MgO interface anisotropies [1, 2]. More recently, shape anisotropies through the use of high aspect ratios between film thickness and device diameter have been explored [3,4] or combinations of interface and shape anisotropies. Both approaches, CoFeB|MgO interface anisotropy dependent and shape anisotropy dependent device designs provide a significant challenge for the reconciliation of fast write times and high retention. Fast and reliably writing devices (<10ns, below 1E-6 write error rate (WER) floor) have typically shown low retention barriers of $E_b < 60k_BT$. When focusing on high retention devices ($E_b > 80k_BT$) using prior free layer designs and materials options reliable and fast writing could not be shown. Here, we present an STT-MRAM free layer material that relies on bulk magnetocrystalline anisotropy as a source of anisotropy. Unlike in prior work [5] using ordered L10 alloys with high Ms of about 850kA/m we are using materials with about 4 times lower magnetization of around 200kA/m. Using these new low moment high perpendicular bulk anisotropy materials allows for simultaneous achievement of high retention and fast and reliable writing.

II. MATERIALS GROWTH AND CHARACTERIZATION:

Achieving high crystalline ordering is crucial for high perpendicular bulk anisotropy low magnetization materials [6]. We achieve high crystalline ordering through control of growth and annealing conditions using commercially available PVD tools. Blanket film analysis is done on films grown on Si/SiO2 substrate wafers. Device structures are integrated from magnetic tunnel junction films integrated in back-end-of line metal levels of CMOS wafers. The ordered alloy materials system appears amorphous as grown based on X-ray diffraction experiments (Fig. 1a). Subsequent annealing at temperatures above about \geq 300°C crystalizes the alloy in its ordered phase and desired (001) texture (Fig. 1a and 1b). A perpendicular moment corresponding to an Ms of about 200kA/m can be measured by VSM once the sample has been exposed to temperatures above its crystallization temperatures (Fig. 1c). The perpendicular anisotropy field of such annealed alloy was

found to be larger than 30 kOe [7]. High resolution TEM images using the High Angle Annular Dark Field method with Z contrast show excellent crystallinity of the magnetic ordered alloys with the expected ordering of different atomic layers (Fig. 1d).



Fig. 1: Blanket film analysis of ordered alloy film. The ordered alloy film thickness is about 15nm and deposited in between 2 MgO layers of about 1nm thickness on an amorphous seed on a Si/SiO₂ wafer. (a) 20 X-ray diffraction intensity as a function of temperature (ramped at 3° C/s). (b) ω -20 X-ray diffraction intensity after temperature ramp up to 600° C. (c) Perpendicular VSM loop of as grown film vs annealed at 400° C for 60 minutes. (d) High Angle Annular Dark Field Image with Z contrast of the ordered alloy showing the arrangement of the atoms in the crystalline lattice. Figure reprinted from [7] with permission (CC-BY-NC 6042791244981).

III. DEVICE INTEGRATION AND PERFORMANCE

Magnetic tunnel junction stacks using high perpendicular bulk anisotropy ordered alloy materials were deposited on CMOS wafers and integrated into 4kb STT-MRAM arrays. Device sizes for given arrays are controlled through lithography and etch processes. Properties for a device with about 39 nm CD are shown in Fig. 2.



Fig. 2: Single device data example (a) hysteresis loop R-H for 39nm device (b) pulse-width-dependence for V_c for the same device as in (a). (c) WER example for single device: pulse width from 100ns to 1ns. Figures reprinted from [7] with permission (CC-BY-NC 6042791244981).

Fig. 2a demonstrates the high coercive fields of more than 8kOe that can be achieved by using low moment high perpendicular bulk anisotropy materials as free layer. The high coercivity is consistent with a measured retention barrier E_b of about 122k_BT which is well above typical application needs of 40-80 k_BT . It is expected that retention of the ordered alloy free layer can be controlled via the free layer material thickness while maintain the same high perpendicular anisotropy field. It was further shown that these high coercivity fields, H_c, and anisotropy fields, H_K, of the material make the devices particularly field insensitive compared to typical CoFeB|MgO interface anisotropy based devices [7]. Fig. 2c represents the typical pulse width dependence of the write voltage of such high anisotropy low moment material devices by looking at shallow write error rate (WER) slopes. Switching down to 2ns pulse width is shown. Deeper WER floors have been demonstrated elsewhere [7].

IV. CONCLUSION

Unique novel STT-MRAM device behavior allowing the extension of the application space of STT-MRAM was demonstrated. Low moment, high anisotropy, ordered-alloy based free layers allow addressing some limitation of CoFeB based free layer devices in terms of high retention and fast write times. Further work on tunneling magneto-resistance (TMR) and write voltages and currents should allow extending the application space of STT-MRAM towards new applications requiring fast writing and high retention.

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REFERENCES

- G. Hu et al., "Spin-transfer torque MRAM with reliable 2 ns writing for last level cache applications," 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2019, pp. 2.6.1-2.6.4, https://doi:10.1109/IEDM19573.2019.8993604.
- [2] D. C. Worledge and G. Hu, Spin-transfer torque magnetoresistive random access memory technology status and future directions, Nature Reviews Electr. Eng. 1, 730–747 (2024). <u>https://doi.org/10.1038/s44287-024-00111-z</u>
- [3] Perrissin, N.; Lequeux, S.; Strelkov, N.; Chavent, A.; Vila, L.; Buda-Prejbeanu, L. D.; Auffret, S.; Sousa, R. C.; Prejbeanu, I. L.; Dieny, B. A highly thermally stable sub-20 nm magnetic random-access memory based on perpendicular shape anisotropy. Nanoscale 2018, 10, 12187, <u>https://doi.org/10.1039/C8NR01365A</u>
- B. Jinnai et al., "High-Performance Shape-Anisotropy Magnetic Tunnel [4] Junctions down to 2.3 nm," 2020 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2020, pp. 24.6.1-24.6.4, https://doi:10.1109/IEDM13553.2020.9371972. B. Jinnai, J. Igarashi, T. Shinoda, K. Watanabe, S. Fukami and H. Ohno, "Fast Switching Down to 3.5 ns in Sub-5-nm Magnetic Tunnel Junctions Achieved by Engineering Relaxation Time," 2021 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2021, pp. 1-4. https://doi:10.1109/IEDM19574.2021.9720509
- [5] T. Kishi et al., Proc. IEDM Tech. Dig. 1 (2008).
- [6] Jeong, J., Ferrante, Y., Faleev, S. et al. Termination layer compensated tunnelling magnetoresistance in ferrimagnetic Heusler compounds with high perpendicular magnetic anisotropy. Nat Commun 7, 10276 (2016). https://doi.org/10.1038/ncomms10276
- [7] M. G. Gottwald et al., "First Demonstration of High Retention Energy Barriers and 2 ns Switching, Using Magnetic Ordered-Alloy-Based STT MRAM Devices," 2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2024, pp. 1-2, https://doi:10.1109/VLSITechnologyandCir46783.2024.10631319