# Ultra-high Efficiency of SOT-MRAMs using MTJs with Strain-induced Magnetic Anisotropy

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**To break through the limits of conventional MRAMs, MTJs with strain-induced magnetic anisotropy (SIMA-MTJs) were proposed as SOT-MRAM cells and proved to be superior to STT-MRAM with perpendicular magnetic anisotropy. This talk reviews the performances including TMR and write-efficiency compared with those of STT-MRAMs.**

***Index Terms*—MRAM, SOT, Strain, Write-efficiency, TMR**

## I. Introduction

STT-MRAMs using MTJs with perpendicular magnetic anisotropy (PMA-MTJs) have been commercialized mainly for embedded Flash-memory replacement where nonvolatility matters. However, the inherent trade-off relationship between critical switching-current ($I_{csw}$) and nonvolatility has been a big obstacle to be applied for working memory replacements where power consumption in active mode matters.

In order to break the trade-off relationships, MTJs with strain-induced magnetic anisotropy (SIMA-MTJs) were proposed as SOT-MRAM cells [1]. In this talk, the write-efficiency and other performances are reviewed by comparing with those of STT-MRAMs.

## II. MTJ Materials and Structure of MTJs with SIMA

Fig.1 shows the schematic drawing and the cross-sectional TEM image of a SIMA-MTJ.

The materials and the structure were the same as those of conventional MTJs with in-plane magnetic anisotropy. Ta-based spin-Hall electrode (SHE) was deposited as the underlayer of the MTJs. CoFeB with magneto-striction constant of about 4E-5 was used as the storage-layer. MTJ stack was etched by ion-beam into MTJ elements with aspect-ratio of 1 to 2. Anisotropic strain was produced in order for the MTJs to have SIMA by the same concept reported before [1].

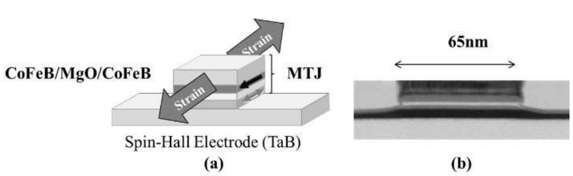


Fig. 1. (a) Structure and materials and (b) cross-sectional TEM image of SIMA-MTJ.

## III. TMR and Nonvolatility of MTJs with SIMA

Reading speed also matters for working memory replacement. However, 150-200% TMR of PMA-MTJs are not enough for the application. The main reason for the limited TMR is due to limited thickness of the storage-layer or insertion of non-magnetic layer in the storage-layer.

### A. Tunneling magneto-resistance(TMR)

There is no thickness limit for the storage-layer of SIMA-MTJs as far as the $I_{csw}$ can be kept small enough for CMOS transistors to be able to supply.

Fig.2(a) shows a hysteresis curve of a patterned SIMA-MTJ with 1.9nm thick storage-layer and 61nm×104nm in size. Over 300% TMR was obtained[2].

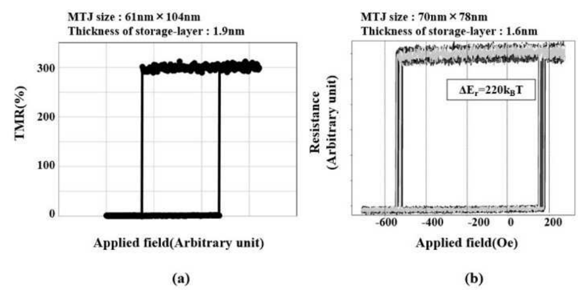


Fig. 2. 300% TMR ratio and the result of repeated hysteresis measurement of SIMA-MTJ

### B. Nonvolatility

Retention energy $\Delta E_r$ was estimated by fitting the switching probability data obtained from repeated resistance-vs-applied magnetic field measurement (RH curves) with the Sharrock's formula [3].

Fig.2(b) shows the repeated R-H curves for a patterned SIMA-MTJ. The MTJ element has large retention energy, $\Delta E_r$, of $220k_BT$. Almost all the energy is thought to come from SIMA.

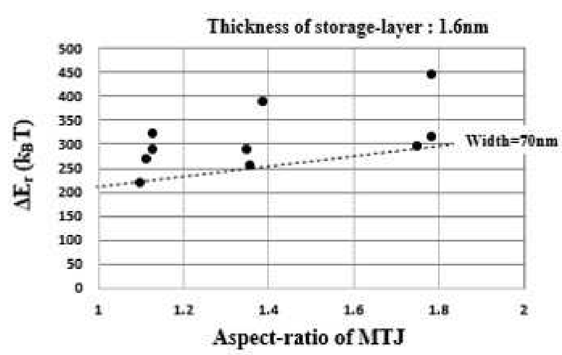


Fig. 3. Aspect-ratio dependence of $\Delta E_r$ of SIMA-MTJs.

Fig.3 shows the aspect-ration dependence of $\Delta E_r$. The dotted extrapolation lines shows that MTJ elements with aspect-ratio of 1 would have large $\Delta E_r$ of larger than 200 $k_BT$. This is a proof of the existence of SIMA.

## IV. SCALABILITY OF NONVOLATILITY(RETENTION ENERGY)

Fig.4 shows the scalability of SIMA-MTJ's retention energy .

The dotted extrapolation lines suggest that even with small size of 20nm, $\Delta E_r$ can be as large as $100k_BT$ to secure 10 years nonvolatility.

The retention energy of SIMA-MTJs is proportional to the width of the MTJs as observed by Fig.4, while that of PMA-MTJs is proportional to the area of the MTJs. Because of this, the retention energy of SIMA-MTJs decrease slower as its size gets smaller than that of PMA-MTJs does. SIMA-MTJs have better scalability in terms of nonvolatility.

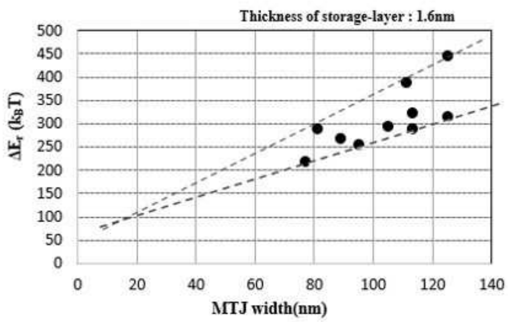


Fig. 4. Scalability of nonvolatility of SIMA-MTJ.

## V. WRITE-EFFICIENCY OF SIMA-MTJS

Here, write-efficiency is defined as $\Delta E_r/I_{csw}$ with write-current pulse width of 10ns.

Fig.5 shows MTJ length dependence of the SOT write-efficiencies of SIMA-MTJs in comparison with those of STT-writing in PMA-MTJs. The smaller the length, the higher the efficiencies for both cases.

For SOT-writing in SIMA-MTJs, very high efficiency of 4.1 $k_BT$ / μA was obtained for MTJs even with large size compared with that for the PMA-MTJs.

At the same size, the efficiency of SIMA-MTJs is about 4 times of those of PMA-MTJs.

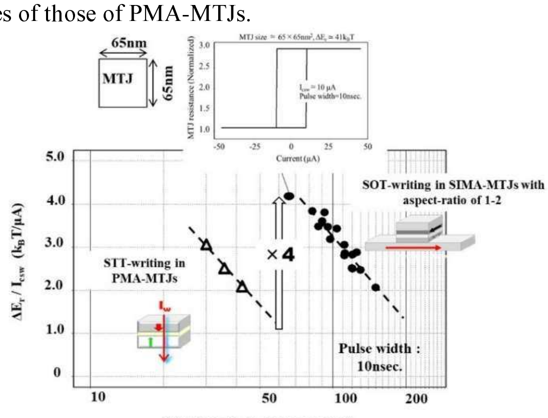


Fig.5. Write-efficiencies and the scalabilities of STT-writing PMA-MTJ and SOT-writing SIMA-MTJ[4] .

## VI. TMR AND WRITE EFFICIENCY IMPROVEMENT TRENDS

Fig.6 shows TMR improvement trend and write-efficiency improvement trend[5].

After the proposal of PMA-MTJs for STT-MRAM with CoFeB/MgO/CoFeB based material in 2005-2008, both TMR and write-efficiency were improved to reach TMR of 200% and write-efficiency of $1k_BT/\mu A$, respectively, in 2008-2010[6].[7],[8].

However, after that there had been almost no improvement reported for about 13-15 years. The development of STT-MRAM technologies seems to reach a deadlock.

In 2023, large TMR of 300% and very high write-efficiency of 4.1 $k_BT/\mu A$ were reported with SOT-MRAM using SIMA-MTJs[2],[4].

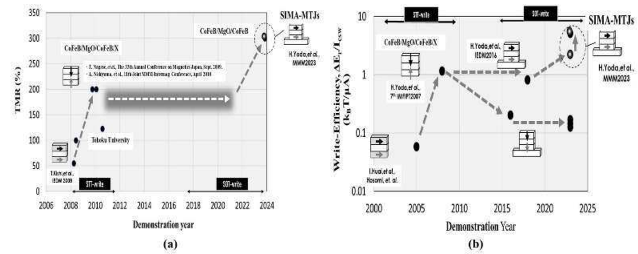


Fig. 6. Improvement history of MRAM. (a) TMR trend, (b) write-efficiency trend[5].

## VII. SUMMARY

Development of SOT-MRAM with SIMA-MTJs was reviewed. The technology has proved much higher write-efficiency and larger TMR than those of PMA-MTJs used in commercialized STT-MRAM.

SOT-MRAM with SIMA-MTJs broke through the trade-off relationships between critical switching-current and nonvolatility to be a promising candidate for cache memory applications of nonvolatile memory.

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