Multi-bit magnetic memory using magnetic multilayer pillars with two-terminal structure

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We investigate magnetization control in a magnetic multilayer pillar on an in-plane magnetized layer using micromagnetic simulations. The multilayer pillar consists of alternating layers possessing or lacking perpendicular magnetic anisotropy. When the bottom layer of the pillar has no perpendicular anisotropy, the magnetization of the pillar bottom is reversed by the spin injection from the in-plane magnetized layer and the spin-polarized current flowing through the pillar. This leads to the formation of a new domain and an accompanying domain wall which generates a new bit pattern. The domain wall is moved by the current. When a pulse current is applied, the magnetization reversal is suppressed, and the domain wall movement is induced. By adjusting the timing of the application of the constant and pulsed currents, magnetic states corresponding to various bit patterns can be realized in the pillar. This multi-bit memory structure operates with only two terminals, and a circuit using multiple pillars is proposed.

***Index Terms*— Magnetic memory, Nonvolatile memory, Spintronics, Numerical simulation**

I. Introduction

Multi-bit memory devices based on domain wall (DW) motion in vertically aligned ferromagnetic nanopillars have been proposed as a promising candidate for high-density memory applications [1]. The DW is moved by a spin-transfer torque (STT) induced by a spin-polarized current (SPC) flowing through the pillar. The magnetization direction in the pillar is read out by a magnetic tunnel junction (MTJ) located at one end of the pillar. A key challenge in realizing such multi-bit memory devices is controlling the magnetization at the opposite end of the pillar.

Micromagnetic simulations of a permalloy pillar have demonstrated a viable writing mechanism. In a structure, an in-plane magnetized layer (IL) is positioned beneath the pillar, and applying a unidirectional current from the top of the pillar through the in-plane layer enables control of the magnetization within the pillar [2]. The number of interconnects is the same as that in the STT-MRAM and fewer than those needed for the spin-orbit-torque (SOT)-MRAM.

In the pillar where the magnetization is aligned along the pillar due to shape anisotropy, the distance between multiple DWs formed within the pillar becomes large, requiring a longer pillar length to store even a single bit of information [2]. In contrast, pillars with perpendicular magnetic anisotropy (PMA) can produce narrower DW spacing, hence, switching the magnetization of the pillar end requires a large SPC [3].

As an alternative pillar structure, magnetic pillars composed of multilayer films of different magnetic materials have been proposed to reduce the DW spacing through DW pinning effects arising from the layered structure [1]. This approach shortens the pillar length required to store a single bit. However, DW writing in such multilayer pillars has not yet been demonstrated. Recent studies have reported that magnetic pillars composed of CoPt multilayers with tunable perpendicular anisotropy can now be fabricated by controlling their composition [4].

In this study, we perform micromagnetic simulations to investigate whether magnetization writing can be achieved and to characterize the behavior of multilayer magnetic pillars under unidirectional current injection control schemes. The goal is to explore the feasibility of applying current-driven control methods with unidirectional current flow to more practical multilayer structures with perpendicular anisotropy.

II. Model and Methods

We considered a cylindrical ferromagnetic pillar with a length of 150 nm along the z-direction and a diameter of 20 nm. The pillar comprised alternating magnetic layers with and without perpendicular magnetic anisotropy (PMA), each with a thickness of 5 nm, forming a multilayer structure. A 5-nm thick IL without PMA was attached to the bottom of the pillar. The magnetization pin layer for the MTJ at the top of the pillar was omitted. The structure was discretized into cubic cells of 1.0 nm^3. The magnetization dynamics of each cell were calculated using the Landau-Lifshitz-Gilbert (LLG) equation including the STT term [2].

The layers with PMA had a perpendicular magnetic anisotropy energy density K_u of 1.0 MJ/m^3, a saturation magnetization M_s of 600 kA/m, and an exchange stiffness constant A of 10 pJ/m. The other layers had K_u of 0.0, M_s of 200 kA/m and A of 2.5 pJ/m. The exchange coupling between the pillar and the IL was set to zero. The direction of the SPC was from the top to the bottom of the pillar. In other words, the direction of the electron flow was from the IL to the top of the pillar. The conversion between the spin current and the SPC was calculated assuming a spin polarizability P of 1.0. As the initial condition in the pillar, a magnetized state along the $-z$-direction was set and then relaxed. The magnetization of the IL was aligned predominantly in-plane due to shape anisotropy. Although we refer to this layer as the IL, its magnetization often pointed obliquely from the in-plane direction, owing to the influence of SPC and dipole-dipole interactions with the pillar.

III. Results and Discussions

We simulated the magnetization control in the pillar whose lower end is composed of 0-K_u layer as shown in Fig. 1(a). The SPC of 5×10^{11} A/m² was applied through the pillar from t = 0 to 3.1 ns. Figure 1 depicts the positions of the DWs in the pillar. First, the magnetization at the bottom of the pillar canted due to the spin injection from the IL (Fig. 1(c)), and then the magnetization at the bottom of the pillar was reversed and a DW was formed at 0.6 ns (Fig. 1(d)). Subsequently, the DW moved upward due to the SPC. In addition, a second DW was formed at approximately 1.2 ns, followed by a third at 1.9 ns and a fourth at 2.6 ns. Each DW continued to move upward (Fig. 1(e)). Then, at 2.9 ns, the first DW reached the top of the pillar and disappeared. At this point, the magnetization pattern consisted of four alternating up and down domains, corresponding to a bit pattern "1010." During the SPC application, the magnetization in the IL underwent canting in different directions. When the SPC was stopped at 3.1 ns, the DW motion ceased, and four DWs stabilized at z = 38 nm, 88 nm, and 127 nm. All these positions were the 0-K_u layers. These results show the successful DW writing in the magnetic multilayer pillar.

Next, we aimed to reproduce a bit pattern in which identical bits appeared in sequence. We created the bit pattern 1001 from the initial pattern 0000. A pulsed SPC was applied after 1.6 ns, in which the SPC was periodically turned on and off with an interval of 0.25 ns, as shown in Fig. 2(a). While the steady SPC was flowing, the magnetization was reversed twice at the bottom of the pillar. As a result, two DWs were formed by 1.6 ns, as shown in Fig. 2(b), (c). At this juncture, the SPC was switched to pulsed SPC with 0.25 ns intervals. When the SPC was turned off, the magnetization at the bottom of the pillar returned to its original direction before the reversal was completed, and the DWs stabilized in the nearby 0-Ku layers (Fig. 2(d)). By repeatedly switching the SPC on and off, only the DWs moved, resulting in the elongation of the domains at the bottom of the pillar. At 2.8 ns, the SPC was switched back to a steady flow, leading to magnetization reversal in the bottom region of the pillar (Fig. 2(e)). When the SPC was turned off at 3.8 ns, the magnetization stabilized into the bit pattern 1001 (Fig. 2(f)). These results demonstrate that the use of pulsed SPC allows for flexible and arbitrary bit pattern formation.

An example of a circuit composed of multiple pillar structures is shown in Fig. 3. As the magnetization state of each pillar can be controlled with just two terminals, it is possible to operate the memory using a circuit in which each pillar is paired with a single control transistor. This suggests that multi-bit memory devices can be controlled using the same number of interconnects as a single-bit STT-MRAM.

Meanwhile, when the bottom layer of the pillar was the layer with K_u = 1.0 MJ/m³, DW writing did not occur, even when an SPC of 1.0×10^{13} A/m² was applied. This indicates that, in multilayer pillar magnetic memory devices, the placement of the 0-Ku layer at the bottom of the pillar, where domains are written, is advantageous because it facilitates DW formation. Compared to our previous study using a permalloy pillar, which achieved 3 bits per 250-nm long [2], the multilayer pillar realized a higher density.

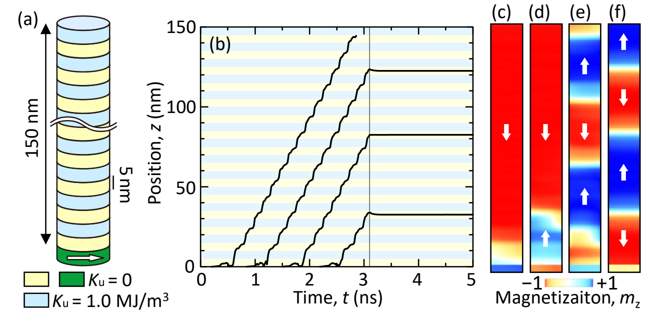

Fig. 1. Continuous and stepwise formation of DWs in the pillar, with the 0-K_u layer (yellow) placed on the IL (green). (a) Structure of the multilayer pillar. (b) DW positions and magnetic configurations at (c) 0.5 ns, (d) 1.0 ns, (e) 2.8 ns, and (f) 5.0 ns. The boundary between the pillar and the IL is z = 0. The white arrows in (c)-(d) indicate the direction of magnetization.

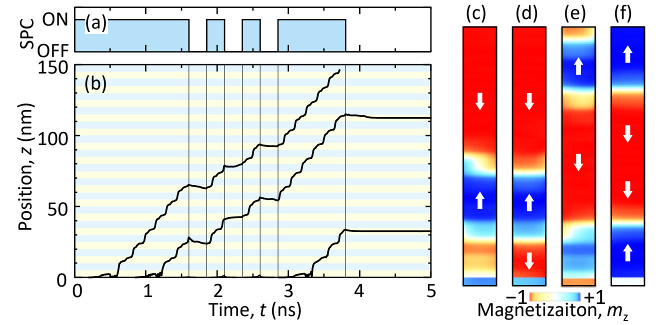

Fig. 2. Formation of the bit pattern 1001 using pulsed SPC. (a) The timing diagram of the applied SPC. (b) DW positions in the pillar. The magnetic structure of the pillar and the IL at t = (c) 1.6 ns, (d) 1.8 ns, (e) 3.7 ns, and (f) 5.0 ns.

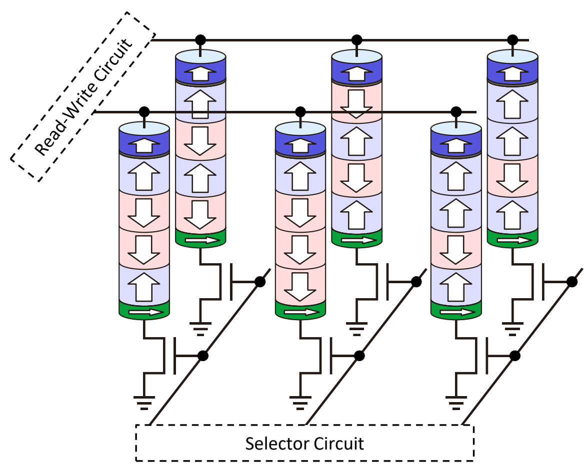

Fig. 3. Circuit comprising six pillars with individual selector transistors.

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